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EXAMINER
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ART UNIT	PAPER NUMBER
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23M1/0403
BLAKELY, SOKOLOFF, TAYLOR AND ZAFMAN
12400 WILSHIRE BOULEVARD, 7TH FLOOR
LOS ANGELES, CA 90025

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

☑ This application has been examined ☐ Responsive to communication filed on _____ ☐ This action is made final.

A shortened statutory period for response to this action is set to expire 3 month(s), 0 days from the date of this letter.
Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☑ Notice of References Cited by Examiner, PTO-892.
2. ☑ Notice of Draftsman's Patent Drawing Review, PTO-948.
3. ☐ Notice of Art Cited by Applicant, PTO-1449.
4. ☐ Notice of Informal Patent Application, PTO-152.
5. ☐ Information on How to Effect Drawing Changes, PTO-1474..
6. ☐ _____.

Part II SUMMARY OF ACTION

1. ☑ Claims 1-36 are pending in the application.
   Of the above, claims 20-36 are withdrawn from consideration.
2. ☐ Claims _____ have been cancelled.
3. ☐ Claims _____ are allowed.
4. ☑ Claims 1-19 are rejected.
5. ☐ Claims _____ are objected to.
6. ☑ Claims 1-36 are subject to restriction or election requirement.
7. ☐ This application has been filed with informal drawings under 37 C.F.R. 1.85 which are acceptable for examination purposes.
8. ☐ Formal drawings are required in response to this Office action.
9. ☐ The corrected or substitute drawings have been received on _____. Under 37 C.F.R. 1.84 these drawings are ☐ acceptable; ☐ not acceptable (see explanation or Notice of Draftsman's Patent Drawing Review, PTO-948).
10. ☐ The proposed additional or substitute sheet(s) of drawings, filed on _____. has (have) been ☐ approved by the examiner; ☐ disapproved by the examiner (see explanation).
11. ☐ The proposed drawing correction, filed _____, has been ☐ approved; ☐ disapproved (see explanation).
12. ☐ Acknowledgement is made of the claim for priority under 35 U.S.C. 119. The certified copy has ☐ been received ☐ not been received ☐ been filed in parent application, serial no. _____; filed on _____.
13. ☐ Since this application apppears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.
14. ☐ Other

EXAMINER'S ACTION

1. This application has been examined.

2. Restriction to one of the following inventions is required under 35 U.S.C. § 121:

I. Claims 1-19, drawn to thermal sensor implemented in microprocessor chip.

II. Claims 20-36, drawn to a microprocessor.

3. The inventions are distinct, each from the other because of the following reasons:

Claims 1-19 call for a thermal sensor which is implemented in an IC chip, especially for a microprocessor. Wherein claims 20-36 call for a structure of the microprocessor in which the thermal sensor can monitor the heat generated and control the operations of the microprocessor.

4. Inventions thermal sensor and integrated circuit chip are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations. (M.P.E.P. § 806.05(c)). In the instant case, the combination as claimed does not require the particulars of the subcombination as claimed because they are distinct to each other. The subcombination has separate utility such as an special integrated circuit chip.

5. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

6. Applicant's election without traverse of claims 1-19 in Examiner Interview Summary Record is acknowledged.

7. Claims 5, 12 and 17 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claims 5, 12 and 17, the phrase of "for each resistor comprising said second resistive element;" is not well defined.

8. The following is a quotation of 35 U.S.C. § 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
>
> Subject matter developed by another person, which qualifies as prior art only under subsection (f) or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

9. Claims 1-19 are rejected under 35 U.S.C. § 103 as being unpatentable over Nelson Pat. No. 4,789,819 in view of Giordano et al. Pat. No. 5,359,236 and Allen and Holdberg, "CMOS Analog Circuit Design".

As per claims 1-3, 8-10 and 15, Giordano et al. disclose an integrated circuit thermal sensor. As shown in Fig. 1A, a portion of a band gap voltage KVbg is applied between the base and emitter of a bipolar transistor Q1, also referred to as the controlled device. Generally, the band gap voltage applied to the base of Q1 is held at a relatively fixed value as a function of temperature, as shown in Fig. 1B. Temperature sensing is achieved by relying on the well known principle that the base-emitter voltage of a bipolar transistor decreases at a predetermined rate as shown in Fig. 1B. Accordingly, Giordano et al. disclose circuits embodying the invention include a means for generating a turn-on signal which increases with increasing temperature. As shown in Figs. 2 and 4, there is shown a temperature dependent current source connected between a power terminal to which is applied a source voltage and a node to which is connected the base of a transistor Q1 and one end of a resistor R2. The net result is that a current IC is supplied to node 14 and a turn-on voltage is generated which increases linearly as a function of increasing temperature. However, Giordano et al. do not call for scaling of the sensing voltage. Such feature is, however, old and well-known in the art. In fact, Nelson discloses a voltage reference circuit including

band-gap reference circuit with breakpoint compensation to adjust the temperature coefficient of the reference voltage as a function of temperature. In the design of an analog integrated circuit, it is necessary to establish a voltage or current reference within the circuit which is substantially independent of variations in temperature. A band gap voltage reference circuit often is utilized to provide such a reference voltage or current. Nelson also discloses a scaling factor so as to obtain an output voltage with nominally zero temperature dependence. This would motivate practitioners in the art to use the voltage scaling as suggested by Nelson into Giordano et al.' integrated circuit thermal sensor to obtain a high resolution of output voltage.

As per claims 4-7, 11-14 and 16-19, Nelson and Giordano et al. disclose the claimed invention except for charge scaling or in other words voltage scaling. It would have been an obvious matter of design choice to use MOSFET transistors coupled with resistive elements to provide a voltage scaling. Moreover, such scaling as claimed in the invention is well-known CMOS technology (see Allen and Holberg, "CMOS Analog Circuit Design", HRW, pp. 539-549, 1987).

10. The prior art made of record and not relied upon is considered pertinent to applicant' disclosure.

[1]	4,779,161	DeShazo, Jr.	Oct. 18, 1988
[2]	4,787,007	Matsumura et al.	Nov. 22, 1988
[3]	4,903,106	Fukunaga et al.	Feb. 20, 1990
[4]	4,935,864	Schmidt et al.	June 19, 1990

[5]	5,087,870	Salesky et al.	Feb. 11, 1992
[6]	5,149,199	Kinoshita et al.	Sept. 22, 1992
[7]	5,170,344	Berton et al.	Dec. 8, 1992
[8]	5,283,631	Koerner et al.	Feb. 1, 1994
[9]	5,325,286	Weng et al.	June 28, 1994

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thai Phan, whose telephone number is (703)305-3812.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist, whose telephone number is (703)305-3800.

Fax communications can be received at (703)305-9724. It is suggested that examiner be informed prior to transmission.

T.P.
Thai Phan
Mar. 28, 1995

KEVIN J. TESKA
SUPERVISORY PATENT EXAMINER
GROUP 2300